CLAIMS

1. (currently amended) A method of forming a contact to a source/drain contact region of a transistor device having a gate, and the source/drain contact region is comprised substantially of silicon, the method comprising:

implanting germanium into a region of the source/drain contact region at a dose ~~not exceeding~~ between 1E13 and 1E17 atoms per centimeter squared using the gate as a mask;

activating the germanium implanted into the source/drain contact region;

implanting ~~a source/drain dopant~~ boron into the source/drain contact, wherein the implanting the ~~source/drain dopant~~ boron is performed subsequent to the activating the germanium; and

forming a nickel silicide over the source/drain contact region after the activating to form the contact.

2. (previously presented) The method of claim 1 wherein the activating the germanium further includes activating the germanium in order to make the germanium substitutional in a lattice of the source/drain contact region, wherein the lattice includes silicon.

3. (previously presented) The method of claim 1 wherein the activating the germanium increases a lattice constant of the lattice in the source/drain contact region.

4 - 6. (canceled)

7. (original) The method of claim 1 wherein the activating includes heating the source/drain contact region to a temperature of greater than 550 C.

8. (original) The method of claim 1 wherein the activating includes heating the source/drain contact region to a temperature of greater than 1000 C.

9. (original) The method of claim 1 wherein the activating further includes heating the source/drain contact region to a temperature in a range of approximately 900 – 1400 C.

10. (original) The method of claim 1 wherein the activating further includes rapid thermal annealing of the source/drain contact region.

11. (original) The method of claim 1 wherein the activating further includes laser annealing of the source/drain contact region.

12. (original) The method of claim 1 wherein the activating further includes arc lamp thermal annealing of the source/drain contact region.

13. (original) The method of claim 1 wherein the activating further includes gas convection annealing of the source/drain contact region.

14. (currently amended) The method of claim 1 wherein the implanting the germanium is performed at a temperature between 25 and 600 degrees Celsius.

15 - 16. (canceled)

17. (previously presented) The method of claim 1 further comprising:

forming a sidewall spacer adjacent to a sidewall of the gate, wherein the implanting the germanium is performed prior to the forming the sidewall spacer.

18. (original) The method of claim 17 wherein the forming the sidewall spacer is performed prior to the implanting the source/drain dopant.

19. (original) The method of claim 1 wherein the gate is over a semiconductor substrate, the source/drain contact region is in the semiconductor substrate, and the source/drain contact region is disposed laterally from the gate.

20. (original) The method of claim 19 further comprising implanting a second source/drain dopant in the semiconductor substrate after the implanting the source/drain dopant, wherein the second source/drain dopant is implanted deeper than the source/drain dopant.

21. (previously presented) The method of claim 19 wherein the implanting the germanium further includes implanting with an energy of at least 3 keV.

22. (previously presented) The method of claim 19 wherein the implanting the germanium further includes implanting with an energy in the range of 3 keV to 50 keV.

23 - 24. (canceled).

25. (original) The method of claim 19 wherein the implanting the particles is performed at a temperature between 25 and 600 degrees Celsius.

26. (currently amended) The method of claim 1, wherein:

the transistor has a second source/drain contact;

the implanting of the further includes implanting the ~~particles~~ germanium into the second source/drain contact region at ~~a dose not exceeding~~ the dose between 1E13 and 1E17 atoms per centimeter squared;

the activating of the germanium further includes activating the germanium ~~of the particles~~ implanted into the second source/drain contact region; and

the implanting ~~of the source/drain dopant~~ boron further includes implanting the ~~source/drain dopant~~ boron into the second source/drain contact region;

further comprising forming a second ~~metal~~ nickel silicide over the second region to form a second contact.

27. (canceled)

28. (original) The method of claim 1, wherein the gate is over a semiconductor substrate and a channel is in the substrate under the gate, further comprising forming a source/drain extension adjacent to the channel in the semiconductor substrate.

29. (canceled)

30. (currently amended) The method of claim 28, wherein the forming comprises:
implanting a second source/drain dopant into the substrate for forming the source/drain extension, wherein the implanting the second source/drain dopant is performed prior to the implanting the ~~source/drain dopant~~ boron.

31. (currently amended) The method of claim 1 further comprising activating the ~~source/drain dopant~~ boron.

32 - 33. (canceled)

34. (currently amended) A method of forming a semiconductor device, the method comprising:
providing semiconductor substrate;
forming a gate over the ~~silicon~~ semiconductor substrate;
implanting germanium into a region of the ~~silicon~~ semiconductor substrate at a dose ~~not exceeding~~ between 1E13 and 1E17 atoms per centimeter squared using the gate using the gate as a mask;
activating the germanium implanted into the region of the semiconductor substrate with a non diffusion activation process;
implanting boron into the region of the semiconductor substrate; and
forming a nickel silicide over the region after the activating.

35. (original) The method of claim 34 wherein the non diffusion activation process includes one of arc lamp rapid thermal annealing of the region and laser annealing of the region.

36. (currently amended) A method of forming a semiconductor device, the method comprising:
forming a gate over a silicon substrate, the substrate having a lattice having a lattice constant;

increasing the lattice constant of the lattice in a source/drain region of the substrate after the forming the gate by implanting germanium at a dose ~~not exceeding~~ between 1E13 and 1E17 using the gate as a mask;

implanting a ~~source/drain dopant~~ boron into the source/drain region, wherein the implanting the ~~source/drain dopant~~ boron is performed subsequent to the increasing the lattice constant; and

forming a nickel silicide over the portion of the source/drain region.

37 - 43. (canceled)

44. (currently amended) A method of forming a semiconductor device, the method comprising:

forming a gate over a silicon semiconductor substrate;

implanting particles including germanium into a region of the substrate after the forming the gate at a dose ~~not exceeding~~ between 1E13 and 1E17 atoms per centimeter squared using the gate as a mask;

activating the germanium implanted into the region;

implanting ~~a source/drain dopant~~ boron into the substrate for forming at least a portion of a source/drain region in the substrate, wherein the implanting the ~~source/drain dopant~~ boron is performed subsequent to the activating the germanium; and

forming a nickel silicide over the region after the activating.

45. (currently amended) In a transistor device structure having a gate stack and source/drain contact regions comprised primarily of a first material, wherein the source/drain contact regions have a lattice constant, a method of forming a contact, comprising:

implanting germanium at a dose ~~not exceeding~~ between 1E13 and 1E17 atoms per centimeter squared into the source/drain contact regions using the gate stack as a mask;

activating the germanium implanted into the source/drain contact regions to increase the lattice constant of the source/drain contact regions;

implanting boron into the source/drain contact regions after the step of activating; and

forming a nickel silicide over the source/drain contact regions after the step of activating ~~of the atoms~~.

46 - 47. (canceled)